Achieving 0.82 dB NF_{min} in High-Drain-Bias GaN HEMTs via Buffer and Field-Plate Engineering for High-Linearity LNA Applications

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***Abstract*— In this letter, minimum noise figure (NF_{min}) of GaN high-electron-mobility transistors (HEMTs) under high-drain bias (V_{DS} > 20V) is investigated and optimized for high-linearity low noise amplifier (LNA) applications. By employing a 1 μm Fe-doped GaN buffer and a non-overlapping source field plate (SFP), the device achieves a NF_{min} of 0.82 dB at 3 GHz and a V_{DS} of 24 V, while delivering an associated gain (G_a) of 16.61 dB and an output third-order intercept point (OIP3) of 31.8 dBm. Experimental comparison and a physics-based noise model identify the sharp increase in gate leakage current (I_G) as the dominant cause of NF_{min} degradation under high V_{DS}, and confirm its suppression using 1 μm Fe-doped buffer scheme. Moreover, a non-overlapping SFP suppresses the device's thermal noise by lowering the intrinsic resistances (R_i, R_{gd}). This work provides a novel design optimization strategy for high-bias, low-noise GaN HEMTs tailored for high-linearity LNA applications.**

***Index Terms*—Buffer, gate leakage current, GaN HEMT, high drain bias, noise figure, source field plate.**

I. Introduction

Low noise amplifiers (LNAs) demanding low noise figure, high linearity, and robustness are increasingly implemented using gallium nitride high-electron-mobility transistors (GaN HEMTs) due to III-N's superior material properties [1], [2], [3]. To improve noise performance, various approaches have been explored in GaN HEMTs, including n^+-GaN source/drain, gate scaling, damage-free etching and thin barrier [4], [5], [6]. However, most existing studies on GaN HEMT noise performance have focused on operation at relatively low drain-source voltage (V_{DS} < 6V), a regime that typically degrades device linearity due to relatively large gate-drain capacitance (C_{gd}). In contrast, increasing V_{DS} may enhance linearity via reduction of C_{gd} [7]. In modern communication systems, high linearity is essentially required in LNAs to withstand high-power signal jamming [8], [9]. Therefore, many GaN LNA monolithic microwave integrated circuits (MMICs) are designed to operate transistors at elevated bias voltages to achieve high linearity [10], [11], [12]. Kobayashi et al. demonstrated a cascode feedback amplifier achieving an output third-order intercept point (OIP3) of 51.9 dBm, and a noise figure of 3 dB at 2 GHz, with each transistor biased at 20 V [10]. Nevertheless, it is a challenge to achieve a low noise figure under high-bias conditions required for high linearity [13], [14]. For instance, it is observed that the NF_{min} of a GaN HEMT at 8 GHz increases from 0.93 dB to 1.75 dB as V_{DS} rises from 4 V to 24 V [13]. This degradation in noise performance at high bias is likely caused by increased gate leakage and enhanced self-heating effect [15], [16]. Thus, buffer engineering and field plate technologies, typically developed to improve high-power RF performance of GaN HEMTs, are expected to achieve low noise, particularly under high-bias conditions. Key techniques include (semi-)insulating GaN buffer and source field plate, to minimize leakage current and smoothen the electric field distribution, respectively [17], [18], [19], [20], [21]. However, their specific impacts on the NF_{min} remain largely unexplored.

In this letter, four devices were comparatively studied to investigate impacts of buffer engineering and field plate technologies on noise performance under high bias. Experimental results demonstrate that the device utilizing a 1 μm Fe-doped buffer and a non-overlapping source field plate maintains excellent noise figure and achieves high linearity at 24 V.

II. Experimental

Devices were fabricated on 6-inch SiC substrates with an epitaxial structure comprising a GaN buffer/channel layer, a 1 nm AlN interlayer, a 20 nm $Al_{0.23}Ga_{0.77}N$ barrier, and a 2 nm GaN cap, as shown in Fig. 1. Devices I and III feature a 0.5 μm unintentionally doped (UID) buffer, while Devices II and IV incorporate a 1 μm Fe-doped buffer with a peak Fe concentration of approximately 1×10^{19} cm^{-3}. Hall measurements yielded a 2DEG sheet density of 8×10^{12} cm^{-2} and a mobility of 2100 $cm^2/V\cdot s$.

Device fabrication commenced with source/drain Si^+ ion implantation. A 100 nm LPCVD SiN layer was deposited prior to source/drain metallization as an annealing sacrificial layer. Ohmic contacts (Ti/Pt/Au) yielded a contact resistance of 0.18 Ω·mm and a sheet resistance of 400 Ω/sq, as measured by TLM. A Pt-based T-gate was formed by e-beam evaporation. The resulting structure features gate-head overhangs of approximately 0.4 μm on the drain side and 0.25 μm on the

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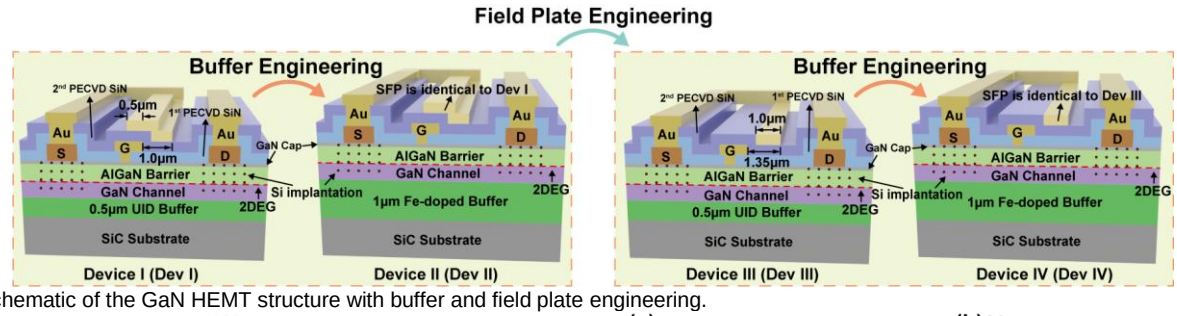

Fig. 1. Schematic of the GaN HEMT structure with buffer and field plate engineering.

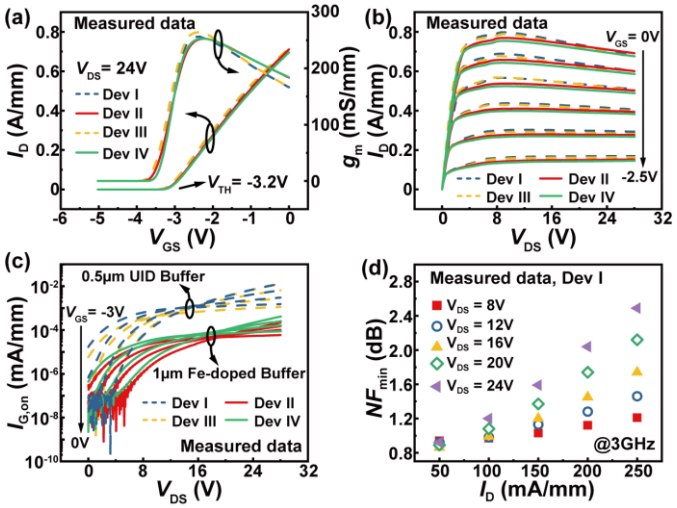

Fig. 2. Characteristics of Devices I-IV: (a) transfer curves, (b) output curves, (c) on-state gate leakage current (I_G), and (d) bias-dependent minimum noise figure (NF_{min}) of Device I.

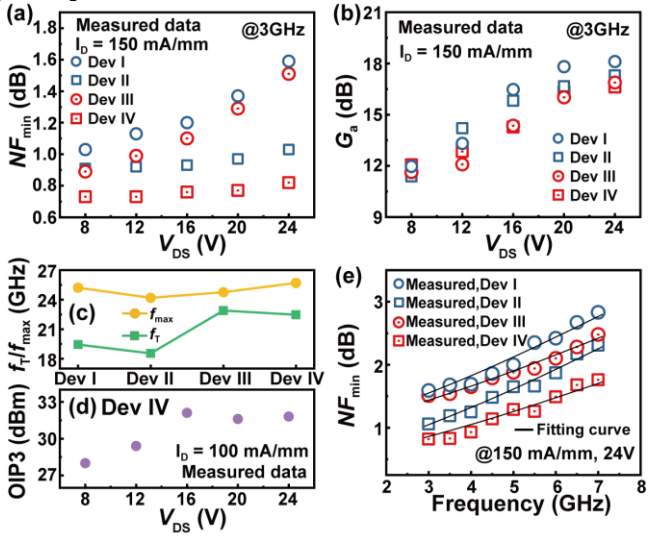

Fig. 3. (a) NF_{min} and (b) associated gain (G_a) vs. V_{DS} at fixed I_D for Devices I-IV. (c) f_T and f_{max} (V_{DS} = 24 V, I_D = 150 mA/mm) for Devices I-IV. (d) OIP3 vs. V_{DS} for Device IV. (e) Frequency dependence of NF_{min} and the corresponding fitting curves for Devices I-IV.

source side. The thicknesses of the first and second PECVD SiN passivation layers are 100 nm and 220 nm, respectively. A 700 nm-thick Ti/Pt/Au metal was deposited as the field plate, which was connected to the source pad.

All devices feature a 0.4 μm L_g, 1 μm L_{gs}, 3.2 μm L_{gd}, and a 2 × 300 μm W_g. Devices I and II both employ a 1.5 μm overlapping SFP, including a 0.5 μm overlap with the gate metal. Devices III and IV utilize a 1.0 μm non-overlapping SFP with a 0.35 μm distance from the gate metal.

III. Results and Discussion

Fig. 2(a) presents the transfer characteristics of Devices I-IV, which show high similarity with a common threshold voltage of ~ -3.2 V, a drain current of ~710 mA/mm at V_{GS} = 0 V, and a peak transconductance of 253 mS/mm at V_{DS} = 24 V. As depicted in Fig. 2(b), Devices I and III, incorporating a 0.5 μm UID buffer, exhibit a more pronounced kink effect in their output characteristics compared to Devices II and IV with a 1 μm Fe-doped buffer. Furthermore, Fig. 2(c) reveals that Devices I and III suffer from a more severe increase in on-state gate leakage (I_G) as V_{DS} increases. Specifically, at V_{GS} = 0 V, the I_G of these devices rises by six orders of magnitude as V_{DS} is increased to 24 V. Conversely, the I_G is suppressed by two orders of magnitude in Devices II and IV, which could be attributed to the incorporation of a 1 μm Fe-doped buffer layer. By employing 1 μm Fe-doped buffer, the reduced gate leakage under high bias could be attributed to the increased buffer resistivity and improved crystalline quality, including the reduction of dislocation density [18], [22], [23], [24].

The minimum noise figure (NF_{min}) was measured using the Y-factor method [25]. As illustrated in Fig. 2(d), the NF_{min} of Device I increases with increasing I_D and V_{DS}. Specifically, at an I_D of 150 mA/mm, the NF_{min} increases from 1.03 dB to 1.59 dB as V_{DS} is raised from 8 V to 24 V. As shown in Fig. 3(a), a comparison between Devices I and II, as well as Devices III and IV, reveals that employing a 1 μm Fe-doped buffer can reduce the NF_{min}, particularly under high bias conditions. Specifically, Device III exhibits an NF_{min} of 1.51 dB, whereas Device IV shows a value of 0.82 dB at 24 V. Furthermore, comparing Devices I and III, as well as Devices II and IV, demonstrates that reducing the overlap of the SFP can decrease the NF_{min}. Device II exhibits an NF_{min} of 1.03 dB, whereas Device IV shows a value of 0.82 dB at 24 V. Fig. 3(b) shows that the G_a of Devices III and IV is slightly lower than that of Devices I and II, which is attributed to the decreased reverse isolation caused by the non-overlapping SFP. Fig. 3(c) shows that Devices III and IV, featuring a non-overlapping SFP, achieve a higher f_T. Specifically, Device IV exhibits an f_T of 22.5 GHz and an f_{max} of 25.7 GHz. Fig. 3(d) shows that the OIP3 of Device IV increases from 27.9 dBm to 31.8 dBm as V_{DS} increases from 8 V to 24 V. Notably, Device IV achieves a substantial 3.9 dB improvement in OIP3 as V_{DS} increases from 8 V to 24 V, with a negligible NF_{min} penalty of only 0.1 dB (Fig. 3(a)). Fig. 3(e) compares the frequency dependence of NF_{min} and the corresponding fitting curves for Devices I-IV. As the frequency increases from 3 GHz to 7 GHz, the NF_{min} of Device IV rises from 0.82 dB to 1.76 dB. Dambrine's method [26] was used to extract the model parameters [Fig. 4(a)] while Fig. 4(b) shows great agreement

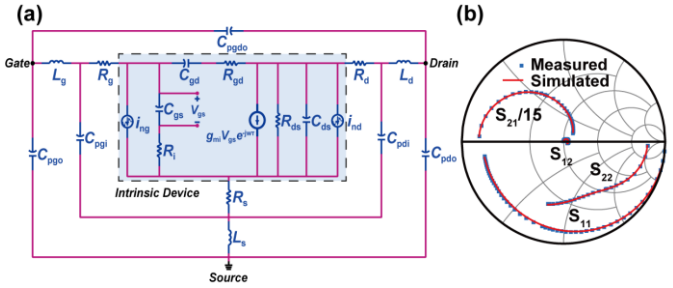

Fig. 4. (a) Small-signal noise equivalent circuit model. (b) Measured and simulated S-parameters from 100 MHz to 10 GHz at 150 mA/mm, 24V with S_{21} scaled by 1/15.

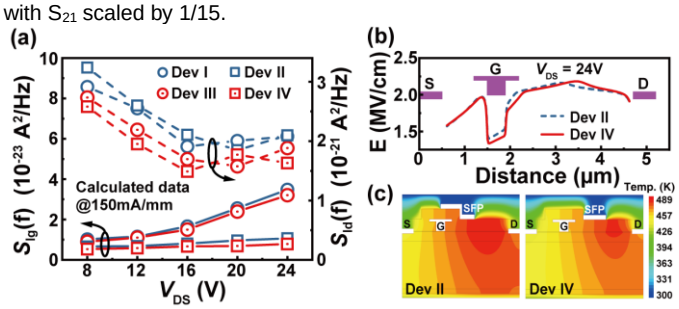

Fig. 5. (a) Noise current power spectral density (S_{Ig}(f)/S_{Id}(f)) extracted from the fitting curves for Devices I-IV. Comparison of Devices II and IV with different field plates in terms of (b) electric field and (c) temperature.

TABLE I
PARTIAL MODEL ELEMENTS OF DEVICES I-IV

Device	C_{pgi} (fF)	C_{gd} (fF)	C_{gs} (pF)	R_i (Ω)	R_{gd} (Ω)	R_{ds} (Ω)	g_{mi} (mS)	τ (pS)
I	178	48.5	1.05	0.89	51.7	421	157	1.70
II	180	50.7	1.07	0.72	54.3	434	165	1.67
III	20.8	74.7	0.99	0.30	29.1	415	158	1.72
IV	24.3	68.1	1.02	0.35	32.0	418	166	1.71

TABLE II
COMPARISON OF NOISE FIGURES OF GAN DEVICES

Param.	[4]	[5]	[30]	[31]	[13]	[14]	**This work**
L_g (μm)	0.05	0.12	0.05	0.25	0.25	0.25	**0.4**
L_{sd} (μm)	0.2	N/A	1.1	5.05	N/A	2.4	**4.6**
f_T (GHz)	230	95	170	43	N/A	38.9	**22.3**
V_{DS} (V)	3	5	3	6	24	20	**24**
I_D (mA/mm)	N/A	250	73	300	54	70	**150**
Freq. (GHz)	30	30	30	3	8	8	**3**
G_a (dB)	8.5	7.7	12	17.5	N/A	N/A	**16.61**
NF_{min} (dB)	0.8	1.3	0.5	1	1.75	0.28	**0.82**

Note: Column of "This work" presents the data extracted from Device IV.

between the simulated and measured S-parameters and noise correlation matrix (C_A) was used to calculate the noise current sources [27]. As shown in Fig. 5(a), the gate (i_{ng}) and drain (i_{nd}) noise current sources represent thermal plus gate shot noise and channel thermal noise, respectively.

Table I lists the extracted small-signal model parameters for Devices I-IV, biased at I_D = 150 mA/mm and V_{DS} = 24 V. Devices I and II exhibit comparable extracted resistances (R_i, R_{gd}, R_{ds}), indicating comparable thermal noise [28]. Consequently, their drain noise current power spectral densities (S_{Id}(f)) are very close, as shown in Fig. 5(a). As V_{DS} increases from 8 V to 24 V, the S_{Id}(f) of Device I gradually decreases from 2.9 × 10^{-21} A^2/Hz to 2.1 × 10^{-21} A^2/Hz, owing to the corresponding increase in the drain-source resistance (R_{ds}) from 142 Ω to 421 Ω [28]. Device II exhibits a similar trend. However, the I_G, which is positively correlated with gate flicker noise, remains suppressed below 10^{-4} mA/mm in Device II as V_{DS} increases to 24 V, whereas that of Device I increases sharply to approximately 10^{-2} mA/mm. This drastic increase directly induces a much faster rise in the gate noise current power spectral density (S_{Ig}(f)) of Device I, which is the primary cause of NF_{min} degradation under high bias. A parallel trend is observed in the comparison between Device III and Device IV.

Compared to Device II with the overlapping SFP, Device IV featuring the non-overlapping SFP exhibits significant improvements in extracted model parameters. Specifically, the intrinsic resistance (R_i) and gate-drain resistance (R_{gd}) decrease from 0.72 Ω to 0.35 Ω and from 54.3 Ω to 32.0 Ω, respectively. As demonstrated by the TCAD simulations in Fig. 5(b) and (c), the non-overlapping SFP shifts the peak electric field toward the drain terminal and reduces the electric field strength in the gate region, thereby mitigating self-heating and reducing the channel temperature beneath the gate. This thermal relief weakens carrier scattering and enhances conductivity, which accounts for the reduced R_i and R_{gd} [29]. Consequently, this mechanism effectively suppresses the S_{Id}(f) of Device III and Device IV, thereby achieving a lower NF_{min}. Concurrently, the non-overlapping SFP reduces the field plate-to-gate metal overlap, significantly lowering the gate-source coupling capacitance (C_{pgi}) as detailed in Table I. This improves the f_T of Device III and Device IV (Fig. 3(c)). Nevertheless, the associated slight increase in gate-drain capacitance (C_{gd}) degrades reverse isolation, leading to a minor reduction in gain for these devices (Fig. 3(b)).

Table II compares the noise figures of state-of-the-art GaN devices. While Ref. [4] leverages ultra-short gate lengths (L_g = 50 nm) to achieve minimal noise figure at high frequencies (>30 GHz), such scaling inherently compromises high-voltage reliability, restricting these devices to low-voltage operation and limiting their utility in high-linearity LNAs. In contrast, our device demonstrates robust operation at 24 V, delivering an excellent NF_{min} of 0.82 dB at 3GHz. With high-voltage and low noise performance, it enables sub-6 GHz high-linearity LNAs and shared-bias integration with GaN PAs. Notably, despite employing a larger L_g than Ref. [31], our work achieves a lower NF_{min} at 3GHz under high bias conditions. Furthermore, compared to Ref. [13] under the same 24 V bias, although our device operates at a higher current density, extrapolation of the noise fitting curves predicts a comparable NF_{min} at 8 GHz. These improvements are primarily attributed to the synergistic optimization of the buffer and field-plate engineering, which effectively suppresses noise figure and ensures high-linearity at high drain bias.

IV. CONCLUSION

To summarize, the implementation of a 1μm Fe-doped buffer combined with a non-overlapping SFP significantly reduced the NF_{min} from 1.59 dB to 0.82 dB at V_{DS} = 24 V. The observed NF_{min} reduction was associated with a reduction in I_G achieved via the 1 μm Fe-doped buffer, a correlation validated by a physics-based noise model. Additionally, the non-overlapping SFP suppresses thermal noise by lowering R_i and R_{gd}, although it slightly reduces gain. This work offers a novel design strategy for implementing high-bias, low-noise GaN HEMTs in high-linearity LNA applications.

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